PATENT
Attorney Docket No. ASC-049C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Fitzgerald		
SERIAL NO.:	10/774,890	GROUP NO.:	2818
FILING DATE:	February 9, 2004	EXAMINER:	Tran, Mai Huong C.
TITLE:	RELAXED SiGe PLATFORM FOR HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLACEMENT SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In response to the Office Action dated July 8, 2005, Applicants hereby re-submit the PTO-1449 filed on October 1, 2004, to correct defects in the header appearing on pages 2, 3, and 4. Applicants request that the Supplemental Information Disclosure Statement now be considered by the Examiner in connection with the examination of the above-identified patent application. Applicants have not resubmitted copies of the references but would be happy to do so upon request.

Respectfully submitted,

Date: August 29, 2005
Reg. No. 44,381

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FORM PTO-1449 **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**	ATTORNEY DOCKET NO.: ASC-049C1 APPLICANT(S): Fitzgerald SERIAL NO.: 10/774,890 FILING DATE: February 9, 2004 GROUP: 2818

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A170	2002/0063292	05/30/2002	Armstrong *et al.*			
	A171	2002/0190284	12/19/2002	Murthy *et al.*			12/30/1999
	A172	2004/0007724	01/15/2004	Murthy *et al.*			07/12/2002
	A173	2004/0014276	01/22/2004	Murthy *et al.*			07/16/2002
	A174	2004/0070035	04/15/2004	Murthy *et al.*			07/23/2003
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	A176	2004/0119101	06/24/2004	Schrom *et al.*			12/23/2002
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	A190	6,743,684	06/01/2004	Liu			10/11/2002

EXAMINER	DATE CONSIDERED

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FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C102	Gannavaram, *et al.*, "Low Temperature (≤800°C) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS," IEEE International Electron Device Meeting Technical Digest, (2000), pp. 137-440.
	C103	Ge *et al.*, "Process-Strained Si (PSS) CMOS Technology Featuring 3D Strain Engineering," IEEE International Electron Devices Meeting Technical Digest, (2003) pp. 73-76.
	C104	Ghani *et al.*, "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," IEEE International Electron Devices Meeting Technical Digest, (2003), 11.6.1-11.6.3.
	C105	Hamada *et al.*, "A New Aspect of Mechanical Stress Effects in Scaled MOS Devices," IEEE Transactions on Electron Devices, Vol. 38, No. 4 (April 1991), pp. 895-900.
	C106	Huang *et al.*, "Isolation Process Dependence of Channel Mobility in Thin-Film SOI Devices," IEEE Electron Device Letters, Vol. 17, No. 6 (June 1996), pp. 291-293.
	C107	Huang *et al.*, "LOCOS-Induced Stress Effects on Thin-Film SOI Devices," IEEE Transactions on Electron Devices, Vol. 44, No. 4 (April 1997), pp. 646-650.
	C108	Huang, *et al.*, "Reduction of Source/Drain Series Resistance and Its Impact on Device Performance for PMOS Transistors with Raised $Si_{1-x}Ge_x$ Source/Drain", IEEE Electron Device Letters, Vol. 21, No. 9, (Sept. 2000) pp. 448-450.
	C109	Iida *et al.*, "Thermal behavior of residual strain in silicon-on-insulator bonded wafer and effects on electron mobility," Solid-State Electronics, Vol. 43 (1999), pp. 1117-1120.

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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C110	Ito *et al.*, "Mechanical Stress Effect on Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design," IEEE International Electron Devices Meeting Technical Digest, (2000), pp. 247-250.
	C111	Lochtefeld *et al.*, "Investigating the Relationship Between Electron Mobility and Velocity in Deeply Scaled NMOS via Mechanical Stress," IEEE Electron Device Letters, Vol. 22, No. 12 (2001), pp. 591-593.
	C112	Ootsuka *et al.*, "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Applications," IEEE International Electron Devices Meeting Technical Digest, (2000), pp. 575-578.
	C113	Ota *et al.*, "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," IEEE International Electron Devices Meeting Technical Digest, (2002), pp. 27-30.
	C114	Öztürk, *et al.*, "Advanced $Si_{1-x}Ge_x$ Source/Drain and Contact Technologies for Sub-70 nm CMOS," IEEE International Electron Device Meeting Technical Digest, (2002), pp. 375-378.
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	C116	Öztürk, *et al.*, "Selective Silicon-Gremanium Source/Drain Technology for Nanoscale CMOS," Mat. Res. Soc. Symp. Proc., Vol. 717, (2002), pp. C4.1.1-C4.1.12.
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OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C119	Thompson *et al.*, "A Logic Nanotechnology Featuring Strained-Silicon," IEEE Electron Device Letters, Vol. 25, No. 4 (April 2004), pp. 191-193.
	C120	Thompson *et al.*, "A 90 nm Logic Technology Featuring 50nm Strained-Silicon Channel Transistors, 7 layers of Cu *Interconnects*, Low k ILD, and 1um^2 SRAM Cell," IEEE International Electron Devices Meeting Technical Digest, (2002), pp. 61-64.
	C121	Tiwari *et al.*, "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," IEEE International Electron Devices Meeting Technical Digest, (1997), pp. 939-941.
	C122	Uchino, *et al.*, "A Raised Source/Drain Technology Using In-situ P-doped SiGe and B-doped Si for 0.1-μm CMOS ULSIs," IEEE International Electron Device Meeting Technical Digest, (1997), pp. 479-482.

EXAMINER	DATE CONSIDERED